Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 4, 5, 13, 14, 21, 22, 30, 31, 39, 40, 47, 48, 55, and 56. Please amend claims 1, 10, 18, 27, 36, 45, 53, and 57, as follows:

Listing of Claims:

1. (Currently amended) A compensation circuit for an adjustable delay circuit having fine and coarse delay circuits, comprising:

a reference delay circuit having an input at which an input clock signal is applied and an output at which a reference delayed clock signal is provided, the reference delay circuit having a reference fine delay component and a reference coarse delay component, the time delay of the coarse delay component greater than the time delay of the fine delay component and having an expected relationship with respect to the time delay of the fine delay component;

an adjustable fine delay circuit having a control terminal at which a control signal is applied, and further having an input at which the input clock signal is applied and an output at which a variable delayed clock signal is provided, the adjustable fine delay circuit having a time delay adjusted according to the control signal;

a phase detector having a first input coupled to the output of the reference coarse delay component ~~circuit~~ and a second input coupled to the output of the adjustable fine delay circuit to compare the phase relationship of the reference delayed clock signal and the variable delayed clock signal, the phase detector generating an output signal indicative of the phase relationship; [[and]]

a feedback circuit coupled to the phase detector to generate a compensation signal indicative of the variance from the expected relationship between the time delay of the coarse and fine delay components based on the output signal from the phase detector~~, the feedback circuit further providing the compensation signal to the adjustable fine delay circuit as the control signal~~; and

a stabilization circuit coupled to the feedback circuit and the adjustable fine delay circuit and configured to generate a stabilized compensation signal provided to the adjustable fine delay circuit as the control signal in response to the compensation signal from the feedback circuit, the stabilization circuit including at least one stabilization stage having a flip-flop coupled to an input of a NOR gate and an inverter coupled to the output of the NOR gate.

2. (Original) The compensation circuit of claim 1 wherein the feedback circuit comprises a shift register storing a binary value, the binary value modified by shifting bits in response to the output signal from the phase detector.

3. (Original) The compensation circuit of claim 2 wherein the shift register comprises a three-bit shift register.

4. (Cancelled)

5. (Cancelled)

6. (Original) The compensation circuit of claim 1 wherein the phase detector comprises:

a latch having inputs coupled to the output of the reference delay circuit and the adjustable fine delay circuit, and further having outputs; and

a buffer circuit coupled to the outputs of the latch to provide an output signal having first and second components to the feedback circuit.

7. (Original) The compensation circuit of claim 1 wherein the coarse delay component of the reference delay circuit comprises a pair of series coupled inverters.

8. (Original) The compensation circuit of claim 1 wherein the reference fine delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference coarse delay component.

9. (Original) The compensation circuit of claim 1 wherein the reference coarse delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference fine delay component.

10. (Currently amended) A compensation circuit for a variable delay circuit, comprising:

an adjustable delay stage having a control input at which a control signal is applied, an input at which a clock signal is applied, and an output at which a variable delay clock signal is provided, the adjustable delay stage having a variable delay adjusted according to the control signal;

a first reference delay stage having an input at which the clock signal is applied and an output at which a delayed clock signal is provided, the first reference delay stage having a first reference time delay;

a second reference delay stage coupled to the first reference delay stage and having an output at which a reference delay clock signal is provided, the second reference delay stage having a second reference time delay with an expected delay relationship to the first reference time delay;

a latch circuit having a first input coupled to the second reference delay stage and a second input coupled to the adjustable delay stage ~~circuit~~ to compare the phase relationship between the reference delay clock signal and the variable delay clock signal, the latch circuit further having first and second outputs at which first and second phase signals indicative of the phase relationship are provided, respectively; [[and]]

a feedback circuit coupled to the first and second outputs of the latch circuit to generate a feedback signal in response to the logic states of the first and second phase signals, the

feedback signal indicative of the variance from the expected delay relationship and provided by the feedback circuit to the adjustable delay stage as the control signal; and

a signal stabilization circuit coupled to the feedback circuit and configured to generate a stabilized feedback signal in response to the feedback signal from the feedback circuit, the stabilization circuit including at least one stabilization stage having a flip-flop coupled to an input of a NOR gate and an inverter coupled to the output of the NOR gate.

11. (Original) The compensation circuit of claim 10 wherein the feedback circuit comprises a shift register storing a binary value, the binary value modified by shifting bits in response to the output signal from the latch circuit.

12. (Original) The compensation circuit of claim 11 wherein the shift register comprises a three-bit shift register.

13. (Cancelled)

14. (Cancelled)

15. (Original) The compensation circuit of claim 10 wherein the latch circuit comprises:

an S-R latch having inputs coupled to the second reference delay stage and the adjustable delay circuit; and

a buffer circuit coupled to outputs of the S-R latch to provide an output signal having first and second components to the feedback circuit.

16. (Original) The compensation circuit of claim 10 wherein the first reference delay stage comprises a reference fine delay stage and the second reference delay stage comprises a reference coarse delay stage.

17. (Original) The compensation circuit of claim 10 wherein the first reference delay stage comprises a reference coarse delay stage and the second reference delay stage comprises a reference fine delay stage.

18. (Currently amended) A delay-locked loop, comprising:

a variable delay line having a fine delay circuit and at least one coarse delay circuit;

a delay controller coupled to the variable delay line for adjusting the time delay of the variable delay line; and

a compensation circuit coupled to the delay controller for adjusting a time delay relationship between the fine delay and the coarse delay circuits of the variable delay line, the compensation circuit comprising,

a reference delay circuit having an input at which an input clock signal is applied and an output at which a reference delayed clock signal is provided, the reference delay circuit having a reference fine delay component and a reference coarse delay component, the time delay of the coarse delay component greater than the time delay of the fine delay component and having an expected relationship with respect to the time delay of the fine delay component;

an adjustable fine delay circuit having a control terminal at which a control signal is applied, and further having an input at which the input clock signal is applied and an output at which a variable delayed clock signal is provided, the adjustable fine delay circuit having a time delay adjusted according to the control signal;

a phase detector having a first input coupled to the output of the reference coarse delay component ~~circuit~~ and a second input coupled to the output of the adjustable fine delay circuit to compare the phase relationship of the reference delayed clock signal and the variable delayed clock signal, the phase detector generating an output signal indicative of the phase relationship; [[and]]

a feedback circuit coupled to the phase detector to generate a compensation signal indicative of the variance from the expected relationship between the time

delay of the coarse and fine delay components based on the output signal from the phase detector, the feedback circuit further providing the compensation signal to the adjustable fine delay circuit as the control signal;

19. (Original) The delay-locked loop of claim 18 wherein the feedback circuit of the compensation circuit comprises a shift register storing a binary value, the binary value modified by shifting bits in response to the output signal from the phase detector.

20. (Original) The delay-locked loop of claim 19 wherein the shift register comprises a three-bit shift register.

21. (Cancelled)

22. (Cancelled)

23. (Original) The delay-locked loop of claim 18 wherein the phase detector of the compensation circuit comprises:

a latch having inputs coupled to the output of the reference delay circuit and the adjustable fine delay circuit, and further having outputs; and

a buffer circuit coupled to the outputs of the latch to provide an output signal having first and second components to the feedback circuit.

24. (Original) The delay-locked loop of claim 18 wherein the coarse delay component of the reference delay circuit comprises a pair of series coupled inverters.

25. (Original) The delay-locked loop of claim 18 wherein the reference fine delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference coarse delay component.

26. (Original) The delay-locked loop of claim 18 wherein the reference coarse delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference fine delay component.

27. (Currently amended) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a delay-locked loop coupled to at least the control circuit and adapted to receive an input clock signal, the delay-locked loop operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the delay-locked loop comprising,

a variable delay line having a fine delay circuit and at least one coarse delay circuit;

a delay controller coupled to the variable delay line for adjusting the time delay of the variable delay line; and

a compensation circuit coupled to the delay controller for adjusting a time delay relationship between the fine delay and the coarse delay circuits of the variable delay line, the compensation circuit comprising,

a reference delay circuit having an input at which the input clock signal is applied and an output at which a reference delayed clock signal is provided, the reference delay circuit having a reference fine delay component and a reference coarse delay component, the time delay of the coarse delay component greater than the time delay of the fine

delay component and having an expected relationship with respect to the time delay of the fine delay component;

an adjustable fine delay circuit having a control terminal at which a control signal is applied, and further having an input at which the input clock signal is applied and an output at which a variable delayed clock signal is provided, the adjustable fine delay circuit having a time delay adjusted according to the control signal;

a phase detector having a first input coupled to the output of the reference coarse delay component ~~circuit~~ and a second input coupled to the output of the adjustable fine delay circuit to compare the phase relationship of the reference delayed clock signal and the variable delayed clock signal, the phase detector generating an output signal indicative of the phase relationship; and

a feedback circuit coupled to the phase detector to generate a compensation signal indicative of the variance from the expected relationship between the time delay of the coarse and fine delay components based on the output signal from the phase detector, the feedback circuit further providing the compensation signal to the adjustable fine delay circuit as the control signal; and

a stabilization circuit coupled to the feedback circuit and the adjustable fine delay circuit and configured to generate a stabilized compensation signal provided to the adjustable fine delay circuit as the control signal in response to the compensation signal from the feedback circuit, the stabilization circuit including at least one stabilization stage having a flip-flop coupled to an input of a NOR gate and an inverter coupled to the output of the NOR gate.

28. (Original) The memory device of claim 27 wherein the feedback circuit of the compensation circuit comprises a shift register storing a binary value, the binary value modified by shifting bits in response to the output signal from the phase detector.

29. (Original) The memory device of claim 28 wherein the shift register comprises a three-bit shift register.

30. (Cancelled)

31. (Cancelled)

32. (Original) The memory device of claim 27 wherein the phase detector of the compensation circuit comprises:

a latch having inputs coupled to the output of the reference delay circuit and the adjustable fine delay circuit, and further having outputs; and

a buffer circuit coupled to the outputs of the latch to provide an output signal having first and second components to the feedback circuit.

33. (Original) The memory device of claim 27 wherein the coarse delay component of the reference delay circuit comprises a pair of series coupled inverters.

34. (Original) The memory device of claim 27 wherein the reference fine delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference coarse delay component.

35. (Original) The memory device of claim 27 wherein the reference coarse delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference fine delay component.

36. (Currently amended) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a delay-locked loop coupled to at least the control circuit and adapted to receive an input clock signal, the delay-locked loop operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the delay-locked loop comprising,

a variable delay line having a fine delay circuit and at least one coarse delay circuit;

a delay controller coupled to the variable delay line for adjusting the time delay of the variable delay line; and

a compensation circuit coupled to the delay controller for adjusting a time delay relationship between the fine delay and the coarse delay circuits of the variable delay line, the compensation circuit comprising,

a reference delay circuit having an input at which the input clock signal is applied and an output at which a reference delayed clock signal is provided, the reference delay circuit having a reference fine delay component and a reference coarse delay component, the time delay of the coarse delay component greater than the time delay of the fine delay component and having an expected relationship with respect to the time delay of the fine delay component;

an adjustable fine delay circuit having a control terminal at which a control signal is applied, and further having an input at which the input clock signal is applied and an output at which a variable delayed clock signal is provided, the adjustable fine delay circuit having a time delay adjusted according to the control signal;

a phase detector having a first input coupled to the output of the coarse delay circuit and a second input coupled to the output of the adjustable fine delay circuit

to compare the phase relationship of the reference delayed clock signal and the variable delayed clock signal, the phase detector generating an output signal indicative of the phase relationship; [[and]]

a feedback circuit coupled to the phase detector to generate a compensation signal indicative of the variance from the expected relationship between the time delay of the coarse and fine delay components based on the output signal from the phase detector, the feedback circuit further providing the compensation signal to the adjustable fine delay circuit as the control signal; and

a stabilization circuit coupled to the feedback circuit and the adjustable fine delay circuit and configured to generate a stabilized compensation signal provided to the adjustable fine delay circuit as the control signal in response to the compensation signal from the feedback circuit, the stabilization circuit including at least one stabilization stage having a flip-flop coupled to an input of a NOR gate and an inverter coupled to the output of the NOR gate.

37. (Original) The computer system of claim 36 wherein the feedback circuit of the compensation circuit comprises a shift register storing a binary value, the binary value modified by shifting bits in response to the output signal from the phase detector.

38. (Original) The computer system of claim 37 wherein the shift register comprises a three-bit shift register.

39. (Cancelled)

40. (Cancelled)

41. (Original) The computer system of claim 36 wherein the phase detector of the compensation circuit comprises:

a latch having inputs coupled to the output of the reference delay circuit and the adjustable fine delay circuit, and further having outputs; and

a buffer circuit coupled to the outputs of the latch to provide an output signal having first and second components to the feedback circuit.

42. (Original) The computer system of claim 36 wherein the coarse delay component of the reference delay circuit comprises a pair of series coupled inverters.

43. (Original) The computer system of claim 36 wherein the reference fine delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference coarse delay component.

44. (Original) The computer system of claim 36 wherein the reference coarse delay component of the reference delay circuit is coupled to receive the input clock signal and provide an output clock signal to the reference fine delay component.

45. (Currently amended) A method for compensating for variance from an expected relationship between a fine delay circuit and a coarse delay circuit of a variable delay line, the method comprising:

delaying an input clock signal by a reference time delay to generate a reference delay clock signal, the reference time delay having a reference fine time delay component and a reference coarse time delay component;

delaying the input clock signal by an adjustable time delay to generate a variable delay clock signal, the adjustable time delay greater than or equal to the reference fine time delay component and less than the reference coarse time delay component;

generating a phase signal indicative of the phase relationship between the reference delay clock signal and the variable delay clock signal;

generating a feedback signal responsive to the phase signal that is indicative of the variance from the expected relationship between the fine delay circuit and the coarse delay circuit;

stabilizing the feedback signal by ignoring transitions of the feedback signal occurring within at least one period of the input clock signal;

adjusting the adjustable time delay according to the stabilized feedback signal to synchronize the phase of the reference delay clock signal and the variable delay clock signal; and

adjusting the relationship between the fine delay circuit and the coarse delay circuit according to the stabilized feedback signal at phase lock.

46. (Original) The method of claim 45 wherein adjusting the adjustable time delay according to the feedback signal comprises activating or deactivating at least one unit fine delay stage of an adjustable fine delay circuit.

47. (Cancelled)

48. (Cancelled)

49. (Original) The method of claim 45 wherein delaying the input clock signal a reference time delay comprises delaying the input clock signal by the reference fine time delay component before delaying the input clock signal by the reference coarse time delay component.

50. (Original) The method of claim 45 wherein delaying the input clock signal a reference time delay comprises delaying the input clock signal by the reference coarse time delay component before delaying the input clock signal by the reference fine time delay component.

51. (Original) The method of claim 45 wherein generating a phase signal comprises generating a phase signal having an up-shift signal and a down-shift signal and wherein generating a feedback signal comprises modifying a binary value by shifting bits according to the up and down shift signals of the phase signal.

52. (Original) The method of claim 45 wherein adjusting the relationship between the fine delay circuit and the coarse delay circuit according to the feedback signal comprises adjusting a point at which the variable delay line switches between a fine delay circuit and a coarse delay circuit when adjusting the delay time of the variable delay line.

53. (Currently amended) A method for compensating for variance from an expected relationship between a fine delay circuit and a coarse delay circuit of a variable delay line, the method comprising:

determining the phase relationship between a reference delay clock signal delayed from an input clock signal by reference time delay and an adjustable delay clock signal delayed from the input clock signal by an adjustable time delay, the reference time delay having a reference fine delay component and a reference coarse delay component;

generating a compensation signal based on the phase relationship between the reference delay clock signal and the adjustable delay clock signal;

stabilizing the compensation signal by ignoring transitions of the compensation signal occurring within at least one period of the input clock signal;

adjusting the adjustable time delay to correct for the phase difference between the reference delay clock signal and the adjustable delay clock signal responsive to the stabilized compensation signal; and

setting the point at which the variable delay line switches from a fine delay circuit to a coarse delay circuit based on the stabilized compensation signal at phase lock to compensate for the variance from the expected relationship.

54. (Original) The method of claim 53 wherein adjusting the adjustable time delay according to the feedback signal comprises activating or deactivating at least one unit fine delay stage of an adjustable fine delay circuit.

55. (Cancelled)

56. (Cancelled)

57. (Currently amended) The method of claim 53 wherein determining the phase relationship between the reference delay clock signal and the adjustable delay clock signal comprises:

delaying the input clock signal by a reference time delay to generate the reference delay clock signal;

delaying the input clock signal by an adjustable time delay to generate the variable delay clock signal; and

generating a phase signal indicative of the phase relationship between the reference delay clock signal and the variable delay clock signal.

58. (Original) The method of claim 57 wherein delaying the input clock signal a reference time delay comprises delaying the input clock signal by the reference fine time delay component before delaying the input clock signal by the reference coarse time delay component.

59. (Original) The method of claim 57 wherein delaying the input clock signal a reference time delay comprises delaying the input clock signal by the reference coarse time delay component before delaying the input clock signal by the reference fine time delay component.

60. (Original) The method of claim 57 wherein generating a phase signal comprises generating a phase signal having an up-shift signal and a down-shift signal and wherein generating the compensation signal comprises modifying a binary value by shifting bits according to the up and down shift signals of the phase signal.